WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor chip having a semiconductor element or an integrated circuit formed in the semiconductor chip, a low dielectric constant insulating film formed on a surface of the semiconductor chip, and a plurality of bump electrodes being provided on the surface of the semiconductor chip;

a wiring board having a plurality of connecting electrodes being electrically connected to the bump electrodes; and

a resin molding filled in a space between the semiconductor chip and the wiring board, the electrically connected bump electrodes and the connecting electrodes being arranged in the space,

wherein the resin molding is formed of a resin having a flux function and changed from liquid to solid when the bump electrodes are in a molten state.

2. A semiconductor device according to claim 1, wherein a relative dielectric constant of the low dielectric constant insulating film is about 3.5 or less.

3. A semiconductor device according to claim 1, wherein an adhesion strength of the low dielectric constant insulating film to each of the semiconductor chip, the insulating film, and a metal film is 15 J/m^2 or less.

4. A semiconductor device according to claim 2, wherein an adhesion strength of the low dielectric constant insulating film to each of the semiconductor chip, the insulating film, and a metal film is 15 J/m^2 or less.

5. A semiconductor device according to claim 1, wherein a coefficient of elasticity of the resin is 20 MPa or more at normal temperature.

6. A semiconductor device according to claim 1, wherein the resin molding comprises a first resin layer close to the semiconductor chip and a second resin layer close to the wiring board, and the second resin layer is a resin layer which does not contain a filler.

7. A semiconductor device according to claim 1, wherein the resin molding comprises a first resin layer close to the semiconductor chip, a second resin layer close to the wiring board, and a third resin layer interposed between the first resin layer and the second resin layer, and the third resin layer is a resin layer which does not contain a filler.

8. A semiconductor device according to claim 1, wherein the bump electrodes of the semiconductor chip are electrically connected to a plurality of connecting electrodes formed on the semiconductor chip, a part of the connecting electrodes are coated with a passivation film comprising at least one layer formed of an organic film.

9. A method of manufacturing a semiconductor device, comprising:

forming a plurality of bump electrodes on a surface of a semiconductor chip, in which a semiconductor element or an integrated circuit is formed, with a low dielectric constant insulating film formed on the surface of the semiconductor chip;

interposing a resin, which has a flux function between the semiconductor chip and a wiring board in which a plurality of connecting electrodes are formed;

aligning the bump electrodes and the respective connecting electrodes with the resin interposed therebetween, and pressing the semiconductor chip and the connecting electrodes against each other; and

heating the semiconductor chip and the wiring board to electrically connect the bump electrodes to the respective connecting electrodes, and to form a resin molding formed of the resin to fill a space between the semiconductor chip and the wiring board,

wherein the resin is a resin which changes from liquid to solid when the bump electrodes are in a molten state in connecting of the bump electrodes to the respective connecting electrodes.

10. A method of manufacturing a semiconductor device according to claim 9, wherein a relative dielectric constant of the low dielectric constant insulating film is about 3.5 or less.

11. A method of manufacturing a semiconductor device, according to claim 9, wherein a coefficient of elasticity of the resin is 20 MPa or more at normal temperature.

12. A method of manufacturing a semiconductor device, according to claim 9, wherein the heating the semiconductor chip and the wiring board is performed in a reflow furnace, and reflow conditions are a temperature of at least 200℃ and a time of at least 60 seconds.

13. A method of manufacturing a semiconductor device, comprising:

forming a plurality of bump electrodes on a surface of a semiconductor chip, in which a semiconductor element or an integrated circuit is formed, with a low dielectric constant insulating film formed on the surface of the semiconductor chip;

interposing a first resin, which has a flux function, in the vicinity of the semiconductor chip, between the semiconductor chip and a wiring board in which a plurality of connecting electrodes are formed;

interposing a second resin, which has a flux functions and contains no filler, in the vicinity of the wiring board, between the semiconductor chip and the wiring board in which the plurality of connecting electrodes are formed;

aligning the bump electrodes and the respective

connecting electrodes with the first and second resins interposed therebetween, and pressing the semiconductor chip and the connecting electrodes against each other; and

heating the semiconductor chip and the wiring board to electrically connect the bump electrodes to the respective connecting electrodes, and to form a resin molding formed of the first and second resins to fill a space between the semiconductor chip and the wiring board,

wherein the first and second resins are resins which change from liquid to solid when the bump electrodes are in a molten state in connecting of the bump electrodes to the respective connecting electrodes.

14. A method of manufacturing a semiconductor device according to claim 13, wherein a relative dielectric constant of the low dielectric constant insulating film is about 3.5 or less.

15. A method of manufacturing a semiconductor device, according to claim 13, wherein a coefficient of elasticity of the resin is 20 MPa or more at normal temperature.

16. A method of manufacturing a semiconductor device, according to claim 13, wherein the heating the semiconductor chip and the wiring board is performed in a reflow furnace, and reflow conditions are a

temperature of at least 200℃ and a time of at least 60 seconds.

17. A method of manufacturing a semiconductor device, comprising:

forming a plurality of bump electrodes on a surface of a semiconductor chip, in which a semiconductor element or an integrated circuit is formed, with a low dielectric constant insulating film formed on the surface of the semiconductor chip;

interposing a first resin, which has a flux function, in the vicinity of the semiconductor chip, between the semiconductor chip and a wiring board in which a plurality of connecting electrodes are formed;

interposing a second resin, which has a flux functions, in the vicinity of the wiring board, between the semiconductor chip and the wiring board in which the plurality of connecting electrodes are formed;

interposing a third resin, which has a flux function and contains no filler, between the first resin and the second resin;

aligning the bump electrodes and the respective connecting electrodes with the first, second and third resins interposed therebetween, and pressing the semiconductor chip and the connecting electrodes against each other; and

heating the semiconductor chip and the wiring board to electrically connect the bump electrodes to

the respective connecting electrodes, and to form a resin molding formed of the first, second and third resins to fill a space between the semiconductor chip and the wiring board,

wherein the first, second and third resins are resins which change from liquid to solid when the bump electrodes are in a molten state in connecting of the bump electrodes to the respective connecting electrodes.

18. A method of manufacturing a semiconductor device according to claim 17, wherein a relative dielectric constant of the low dielectric constant insulating film is about 3.5 or less.

19. A method of manufacturing a semiconductor device, according to claim 17, wherein a coefficient of elasticity of the resin is 20 MPa or more at normal temperature.

20. A method of manufacturing a semiconductor device, according to claim 17, wherein the heating the semiconductor chip and the wiring board is performed in a reflow furnace, and reflow conditions are a temperature of at least 200℃ and a time of at least 60 seconds.